

## CLAIMS

What is claimed is:

- 1    1.    A content addressable memory (CAM) device comprising:  
2        a first plurality of CAM cells each including a first static storage circuit to store a first data  
3            value;  
4        a first pair of bit lines coupled to the first plurality of CAM cells; and  
5        a first sense amplifier including a first transistor having first and second terminals coupled  
6            to first and second bit lines, respectively, of the first pair of bit lines.
- 1    2.    The CAM device of claim 1 wherein the first sense amplifier further includes a second  
2        transistor having first and second terminals coupled to the first and second bit lines,  
3        respectively.
- 1    3.    The CAM device of claim 2 wherein the first sense amplifier further includes a third  
2        transistor having a first terminal and wherein the first and second transistors have  
3        respective third terminals coupled to one another and to the first terminal of the third  
4        transistor.
- 1    4.    The CAM device of claim 3 wherein the third transistor has a second terminal coupled to  
2        receive a control signal and a third terminal coupled to a reference voltage node, the third  
3        transistor being switched to a conducting state in response to the control signal to enable  
4        the first and second transistors to affect states of the first and second bit lines.
- 1    5.    The CAM device of claim 1 wherein the first terminal of the first transistor is a control  
2        terminal, and the second terminal of the second transistor is a control terminal.

1 6. The CAM device of claim 5 wherein the second terminal of the first transistor is an output  
2 terminal, and the first terminal of the second transistor is an output terminal.

1 7. The CAM device of claim 1 wherein the first terminal of the first transistor is a gate  
2 terminal and the second terminal of the first transistor is a drain terminal.

1 8. The CAM device of claim 7 wherein the first sense amplifier further includes a second  
2 transistor having a gate terminal coupled to the second bit line and a drain terminal coupled  
3 to the first bit line.

1 9. The CAM device of claim 1 wherein the first static storage circuit comprises first and  
2 second inverters having respective input and output nodes, the output node of the first  
3 inverter being coupled to the input node of the second inverter and the output node of the  
4 second inverter being coupled to the input node of the first inverter.

1 10. The CAM device of claim 1 wherein the first pair of bit lines is coupled to the first static  
2 storage circuit within each of the first plurality of CAM cells.

1 11. The CAM device of claim 10 wherein the first static storage circuit comprises first and  
2 second access-enable transistors, the first access-enable transistor being coupled between  
3 the input node of the first inverter and a first bit line of the first pair of bit lines, and the  
4 second access-enable transistor being coupled between the input node of the second  
5 inverter and a second bit line of the first pair of bit lines.

1 12. The CAM device of claim 11 further comprising a first word line coupled to control

2 terminals of the first and second access-enable transistors.

1 13. The CAM device of claim 1 further comprising a pair of compare lines coupled to the first  
2 plurality of CAM cells, and wherein each of the first plurality of CAM cells includes a  
3 compare circuit coupled to the pair of compare lines and to the first static storage circuit.

1 14. The CAM device of claim 13 wherein each of the first plurality of CAM cells further  
2 includes a second static storage circuit coupled to the compare circuit of the CAM cell and  
3 configured to store a second data value.

1 15. The CAM device of claim 14 wherein the second data value is a mask value and wherein  
2 the compare circuit includes at least one mask transistor coupled to receive the mask value  
3 from the second static storage circuit.

1 16. The CAM device of claim 14 further comprising a plurality of match lines and wherein the  
2 compare circuit of each CAM cell includes first and second transistors coupled in series  
3 between a reference voltage node and a respective one of the plurality of match lines, and  
4 third and fourth transistors coupled in series between the reference voltage node and a  
5 respective one of the plurality of match lines, wherein a control terminal of the first  
6 transistor is coupled to the first static storage circuit and a control terminal of the third  
7 transistor is coupled to the second static storage circuit.

1 17. The CAM device of claim 14 wherein the second transistor is coupled to a first compare  
2 line of the pair of compare lines and the fourth transistor is coupled to a second compare  
3 line of the pair of compare lines.

1 18. The CAM device of claim 1 further comprising:  
2 a second pair of bit lines;  
3 a first transistor coupled between a first bit line of the first pair of bit lines and a first bit  
4 line of the second pair of bit lines; and  
5 a second transistor coupled between a second bit line of the first pair of bit lines and a  
6 second bit line of the second pair of bit lines.

1 19. The CAM device of claim 18 further comprising:  
2 a second plurality of CAM cells;  
3 a third pair of bit lines coupled to the second plurality of CAM cells;  
4 a third transistor coupled between a first bit line of the third pair of bit lines and the first bit  
5 line of the second pair of bit lines; and  
6 a fourth transistor coupled between a second bit line of the third pair of bit lines and the  
7 second bit line of the second pair of bit lines.

1 20. The CAM device of claim 19 wherein the CAM device further comprises a second sense  
2 amplifier coupled to the third pair of bit lines.

1 21. The CAM device of claim 20 wherein the second sense amplifier comprises a first  
2 transistor having first and second terminals coupled to the first and second bit lines,  
3 respectively, of the third pair of bit lines.

1 22. The CAM device of claim 18 further comprising a second sense amplifier coupled to the  
2 second pair of bit lines.

- 1 23. The CAM device of claim 22 wherein the second sense amplifier comprises a first  
2 transistor having first and second terminals coupled to the first and second bit lines,  
3 respectively, of the second pair of bit lines.
- 1 24. The CAM device of claim 1 wherein the first sense amplifier further includes second and  
2 third transistors, the first terminal of the first transistor being coupled to the first bit line  
3 via the second transistor, and the second terminal of the first transistor being coupled to the  
4 second bit line via the third transistor.
- 1 25. The CAM device of claim 24 wherein the first sense amplifier further includes a fourth  
2 transistor having a first and second terminals, the first terminal of the fourth transistor  
3 being coupled to the second bit line via the third transistor, and the second terminal of the  
4 fourth transistor being coupled to the first bit line via the second transistor.
- 1 26. The CAM device of claim 25 wherein the first and fourth transistors have respective third  
2 terminals coupled to one another.
- 1 27. A content addressable memory (CAM) device comprising:  
2 a plurality of CAM cell groups each including a respective plurality of CAM cells;  
3 a plurality of pairs of group bit lines, each pair of group bit lines being coupled to the  
4 plurality of a CAM cells of a respective one of the CAM cell groups;  
5 a plurality of group sense amplifiers coupled respectively to the plurality of pairs of group  
6 bit lines; and  
7 at least one compare line coupled to the plurality of CAM cells in each of the plurality of  
8 CAM cell groups.

1 28. The CAM device of claim 27 further comprising a pair of column bit lines coupled to each  
2 pair of group bit lines by a respective pair of group-access transistors.

1 29. The CAM device of claim 28 further comprising a column sense amplifier coupled to the  
2 pair of column bit lines.

1 30. The CAM device of claim 28 wherein each of the plurality of CAM cells of a CAM cell  
2 group comprises:  
3 a storage element;  
4 a compare circuit coupled to the storage element; and  
5 a pair of storage-access transistors coupled between the storage element and the pair of  
6 group bit lines coupled to the plurality of CAM cells of the CAM cell group.

1 31. The CAM device of claim 30 further comprising a plurality of row word lines coupled to  
2 control terminals of the storage-access transistors, and a plurality of group word lines  
3 coupled to control terminals of the group-access transistors.

1 32. The CAM device of claim 31 further comprising:  
2 a first decoder circuit to activate one of the plurality of row word lines indicated by a first  
3 portion of an address value; and  
4 a second decoder circuit to activate one of the plurality of group word lines indicated by a  
5 second portion of the address value.

1 33. The CAM device of claim 32 further comprising a control circuit to output a first decode-  
2 enable signal to the first decoder circuit and to output a second decode-enable signal to the

3 second decoder circuit, the first decoder circuit being configured to activate the one of the  
4 plurality of row word lines in response to the first decode-enable signal, and the second  
5 decoder circuit being configured to activate the one of the group word lines in response to  
6 the second decode-enable signal.

1 34. The CAM device of claim 33 wherein the control circuit is configured to output the first  
2 decode-enable signal and second decode-enable signals at different times.

1 35. A method of operation within a content addressable memory (CAM) device, the method  
2 comprising:  
3 switchably forming a path between a static storage circuit of a CAM cell and a first bit line  
4 to reduce a voltage of the first bit line to a first level; and  
5 sinking current within a first sense amplifier coupled to the first bit line to reduce the  
6 voltage of the first bit line to a second level that is lower than the first level.

1 36. The method of claim 35 wherein switchably forming a path between a static storage circuit  
2 and a first bit line comprises activating a word line coupled to a control terminal of a first  
3 transistor, the first transistor being coupled between the first bit line and the static storage  
4 circuit.

1 37. The method of claim 35 wherein switchably forming a path between a static storage circuit  
2 and a first bit line comprises switchably forming a path between a first output node of the  
3 static storage element and the first bit line, the method further comprising switchably  
4 forming a path between a second output node of the static storage element and a second bit  
5 line, the second output node having a higher voltage level than the first output node such

6       that the voltage of the first bit line is reduced to a lower level than the voltage of the second  
7       bit line.

1   38.   The method of claim 35 further comprising outputting an enable signal to the first sense  
2       amplifier to enable the first sense amplifier to sink current.

1   39.   The method of claim 35 wherein the first sense amplifier comprises a first transistor having  
2       a drain terminal coupled to the first bit line, a source terminal coupled to a first node, and a  
3       gate terminal coupled to a second bit line, the first transistor drawing current from the first  
4       bit line when a voltage on the second bit line is higher than the first level.

1   40.   The method of claim 39 wherein the first sense amplifier further comprises a second  
2       transistor having a drain terminal coupled to the first node, a source terminal coupled to a  
3       reference voltage node and a gate terminal coupled to receive an enable signal, the second  
4       transistor forming a path between the first node and the reference voltage node in response  
5       to the enable signal.

1   41.   The method of claim 35 further comprising switchably forming a path between the first bit  
2       line and a second bit line to reduce a voltage of the second bit line to a third level.

1   42.   The method of claim 41 further comprising sinking current within a second sense amplifier  
2       coupled to the second bit line to reduce the voltage of the second bit line to a fourth level  
3       that is lower than the third level.

1   43.   A method of operation within a content addressable memory (CAM) device, the method  
2       comprising:



3 enabling a write driver to draw current from a first bit line to reduce a voltage of the first  
4 bit line from a precharged level to a first reduced level;  
5 enabling a sense amplifier to draw current from the first bit line to reduce the voltage of the  
6 first bit line from the first reduced level to a second reduced level; and  
7 switchably forming a path between the first bit line and a static storage circuit of a CAM  
8 cell to enable the second reduced level of the first bit line to switch the static storage  
9 circuit from a first state to a second state.

1 44. The method of claim 43 wherein enabling the sense amplifier to draw current from the first  
2 bit line comprises enabling the sense amplifier to draw current from the first bit line after  
3 enabling the write driver to draw current from the first bit line.

1 45. The method of claim 43 wherein enabling the write driver to draw current from the first bit  
2 line comprises outputting a write enable signal to the write driver, and wherein enabling the  
3 sense amplifier to draw current from the first bit line comprises outputting a sense enable  
4 signal to the sense amplifier.

1 46. The method of claim 45 wherein switchably forming a path between the first bit line and a  
2 static storage circuit of a CAM cell comprises switchably forming the path between the  
3 first bit line and the static storage circuit after outputting the write enable signal and the  
4 sense enable signal.

1 47. The method of claim 43 wherein enabling the sense amplifier to draw current from the first  
2 bit line comprises enabling the sense amplifier to draw current from the first bit line after  
3 enabling the write driver to draw current from the first bit line, the combined current drawn

4 by the write driver and sense amplifier acting to reduce the first bit line to the second  
5 reduced level.

1 48. A content addressable memory (CAM) device comprising:

2 a CAM cell having static storage means for static storage of a data value;

3 a first bit line;

4 means for switchably forming a path between the static storage means and the first bit line

5 to reduce a voltage of the first bit line to a first level; and

6 a first sense amplifier coupled to the first bit line and having means for drawing current

7 from the first bit line to reduce the voltage of the first bit line to a second level that is

8 lower than the first level.

1 49. The CAM device of claim 48 further comprising:

2 a second bit line; and

3 means for switchably forming a path between the first bit line and a second bit line to

4 reduce a voltage of the second bit line to a third level.

1 50. The CAM device of claim 49 further comprising a second sense amplifier having means for

2 drawing current from the second bit line to reduce the voltage of the second bit line to a

3 fourth level that is lower than the third level.

1 51. A content addressable memory (CAM) device comprising:

2 a CAM cell having static storage means for static storage of a data value;

3 a first bit line;

4 write driver means for drawing current from the first bit line during a first interval to

5           reduce a voltage of the first bit line to a first reduced level;

6           sense amplifier means for drawing current from the first bit line during a second interval to

7           reduce the voltage of the first bit line to a second reduced level, the second interval

8           beginning after the first interval and being at least partially encompassed by the first

9           interval; and

10          means for forming a path between the first bit line and the static storage means.